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PART IV — Offset and drift in operational amplifiers.

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OPERATIONAL AMPLIFIERS, PART IV

Offset and drift in operational amplifiers

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In our previous articles, Operational Amplifiers — Parts I and II it was erroneously stated that the effect of voltage source drift and noise is increased when the summing or source impedance exceeds the open loop input impedance of an operational amplifier. This depends on the equivalent circuit which applies to the published specifications. In this article the correct equivalent circuit is given for the offset parameters and it is shown that closed loop drift performance is completely independent of the value for open loop input impedance regardless of the relative values for the summing and feedback impedance in any amplifier configuration. We regret our previous error and we hope this article will clarify any confusion on this subject.

INTRODUCTION

One of the most fundamental limitations of DC amplifiers, including operational amplifiers, is offset drift. This article will discuss the precise meaning of open loop offset specifications as given by operational amplifier manufacturers and will give equivalent circuits which can be used to predict closed loop offset behavior.

An ideal operational amplifier would have exactly zero output for zero input. This is never quite the case in practice where an amplifier will exhibit some output for zero input signal. The output may include random and spurious AC signals which are generally called noise and a DC signal which is called offset. It is customary in specifying these signals to refer them to the input so that they are then independent of the amplifier's gain. Input offset is then defined as the input required to zero the DC component of the output with zero input signal.

A fixed input offset is usually not a problem since biasing circuits can be devised to cancel this signal. However, changes in input offset due to variations of ambient temperature, supply voltage and component values with time introduces a basic measuring error, since these offset changes cannot be distinguished from changes of input signal. It is customary to refer to changes of offset as "drift". Remember that drift differs from offset in that drift relates the coefficient of offset change either in uV/°C or, uV/day or uV/V; whereas offset refers to the magnitude of voltage (or current as the case may be) required to zero the output at a given temperature, time and supply voltage.

Actually, offset drift can be considered another form of noise which occurs at very low frequencies. Although this article will be primarily confined to a discussion of offset and drift, the equivalent circuits given and many of the conclusions drawn apply to higher frequency noise as well.

EQUIVALENT CIRCUIT FOR OFFSET OF SINGLE-ENDED AMPLIFIER

Figure 1 shows an equivalent circuit which can be used to explain the offset behavior of a single-ended operational amplifier. Remember that an equivalent circuit is only a model and the test of its validity is, 1) does it explain the observed performance of the amplifier and 2) do the coefficients used in the model correspond to those which are measured and published for the amplifier. From empirical observations it is found that for relatively low values of circuit impedances in the external feedback networks the magnitude of input offset is almost independent of the impedances used. However, for large values of feedback impedances, input offset increases almost proportional to the magnitude of the impedances used. To explain this effect it is necessary to include both an offset voltage and offset current source in the equivalent circuit as shown in Figure 1.

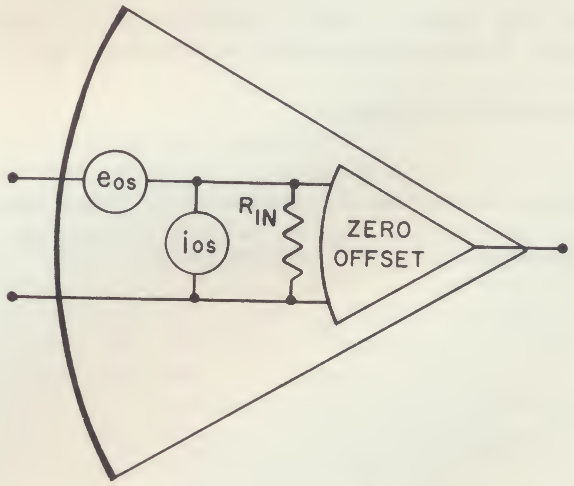


Fig. 1 — Equivalent Circuit For Single-Ended Amplifier

The voltage offset source, e_{OS}, is defined as the voltage required at the input to zero the amplifier output assuming zero source impedance. The current offset source, i_{OS}, is defined as the current required

at the input to zero the output assuming infinite source impedance. R_{IN} represents the open loop input impedance (between inputs) measured under null conditions, that is, very small input signals. The amplifier following the equivalent input circuit would be ideal to the extent of having zero offset and infinite input impedance, but it would have finite gain and bandwidth.

The primary factors contributing to offset voltage may be expressed by the following equation:

$$e_{os} = E_{os} + \frac{\Delta e_{os}}{\Delta T}\Delta T^{+} \frac{\Delta e_{os}}{\Delta V^{+}}\Delta V^{+} + \frac{\Delta e_{os}}{\Delta V^{-}}\Delta V^{-} + \frac{\Delta e_{os}}{\Delta t}\Delta t$$

where,

1. E_{os} is the initial offset voltage usually measured at 25° C ambient with nominal power supply voltages.
2. $\Delta e_{os}/\Delta T$ is the temperature drift coefficient usually given in uV / ° C averaged over some specified temperature range.
3. $\Delta e_{os}/\Delta V^{+}$ and $\Delta e_{os}/\Delta V^{-}$ are the supply voltage drift coefficients for both positive and negative supplies. Normally only one value is given, either in uV/% or uV/V, for whichever coefficient is larger and assuming that only one supply voltage is changed at a time. For most operational amplifiers the positive coefficient is considerably greater and hence is the value specified.
4. $\Delta e_{os}/\Delta t$ is the drift coefficient vs. time usually given in uV/day.

Likewise, the primary factors contributing to offset current may be expressed by the following equation:

$$i_{os} = I_{os} + \frac{\Delta i_{os}}{\Delta T}\Delta T + \frac{\Delta i_{os}}{\Delta V^{+}}\Delta V^{+} + \frac{\Delta i_{os}}{\Delta V^{-}}\Delta V^{-} + \frac{\Delta i_{os}}{\Delta t}\Delta t$$

where the current offset coefficients are defined similarly to the voltage offset coefficients above.

CLOSED LOOP OFFSET BEHAVIOR

The preceding equivalent circuit and definitions may now be applied to predict offset behavior in a closed loop circuit. Let us take as an example the simple inverting amplifier in Figure 2.

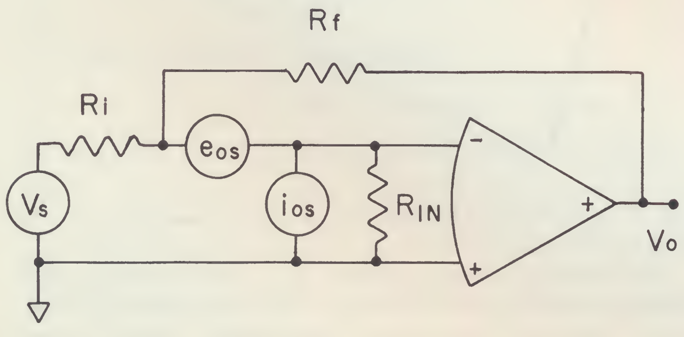


Fig. 2 — Simple Inverting Amplifier

In this circuit it is most revealing to refer the voltage and current offset errors to the source voltage, V_s, as shown in Figure 3.

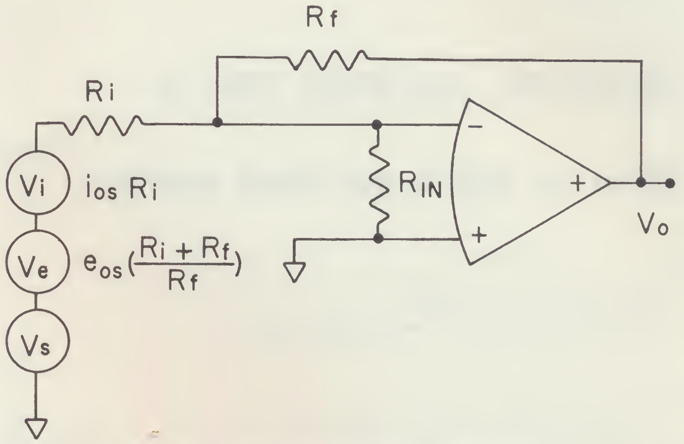


Fig. 3 — Offset Errors Referred To Source Voltage

Total error due to offset referred to the source voltage is then,

$$\Delta V_s = i_{os}R_i + e_{os}\frac{R_i + R_f}{R_f}$$

Offset can be referred to the output by multiplying by closed loop gain as follows:

$$V_o = \left[-\frac{R_f}{R_i}V_s - i_{os}R_f - e_{os}\frac{R_i+R_f}{R_i}\right]\left[\frac{1}{1+\frac{1}{A}\left(1+\frac{R_f}{R_i \parallel R_{IN}}\right)}\right]$$

where A is open loop voltage gain.

Several important conclusions can be drawn from the above analysis:

1. Finite open loop input impedance, R_{IN}, has absolutely no effect on voltage and current offset referred to the source voltage regardless of how large R_i and R_f may be compared to R_{IN}. Referred to the output R_{IN} has only a second order effect inasmuch as it contribures to gain error, but the signal to noise ratio at the output is uneffected by R_{IN} since both signal and offset error are multiplied by the same gain error.

2. Voltage offset referred to the source voltage is multiplied by the factor $(R_i+R_f)/R_f$ to account for the voltage division between R_i and R_f. Thus for low values of closed loop gain (R_f/R_i) the effect of voltage offset is increased by as much as a factor of two at unity closed loop gain.

3. The effect of current offset referred to the source voltage can be obtained by assuming all of the offset current is supplied by the source voltage generating a voltage drop i_{os} R_i. Actually offset current is supplied both from the output and the source voltage in ratios depending on R_i and R_f. But the portion supplied by the output must be divided by closed loop gain to be referred to the input, which yields the same result as if all offset current were supplied by the input.

$$V_i = i_{os} \underbrace{\frac{R_f}{R_i+R_f} R_i}_{\text{supplied by input}} + \underbrace{i_{os} \frac{R_i}{R_i + R_f} R_f \frac{R_i}{R_f}}_{\text{supplied by output}} = i_{os} R_i$$

4. The relative importance of voltage and current offset depends on the magnitude of R_i. Considering offset drift due to temperature only, the temperature coefficent referred to the source voltage would be,

$$\frac{\Delta V_s}{\Delta T} = \frac{\Delta e_{os}}{\Delta T} \frac{R_i + R_f}{R_f} + \frac{\Delta i_{os}}{\Delta T} R_i$$

If we take the example of an amplifier with drift coefficients of 20uV/°C and 1na/°C, we can construct the table in Figure 4 showing input drift $\Delta V_s/\Delta T$ versus input impedance, R_i. (Assuming $R_f >> R_i$.)

R_i	$\Delta e_{os}/\Delta T$	$R_i \Delta i_{os}/\Delta T$	$\Delta V_s/\Delta T$
1K	20uV/°C	1uV/°C	21uV/°C
2K	20uV/°C	2uV/°C	22uV/°C
5K	20uV/°C	5uV/°C	25uV/°C
10K	20uV/°C	10uV/°C	30uV/°C
20K	20uV/°C	20uV/°C	40uV/°C
50K	20uV/°C	50uV/°C	70uV/°C
100K	20uV/°C	100uV/°C	120uV/°C

Fig. 4 — Drift vs. Input Impedance

Note that for R_i=20K ohms, the contributions due to voltage drift and current drift are equal. For R_i < 20 K ohms, drift performance is due primarily to voltage drift, being nearly independent of the value for R_i. For R_i>20K ohms, drift is due primarily to current drift, increasing almost proportional to R_i.
Since the closed loop input impedance of the inverting amplifier is equal to R_i, we see that large input impedance can be obtained only at the expense of offset errors for

$$R_i > \frac{\Delta e_{os}}{\Delta T} \Big/ \frac{\Delta i_{os}}{\Delta T}$$

Example: Let us illustrate these results by a sample calculation of offset errors for the inverting amplifier in Figure 2.

Problem: Input Voltage (V_s) = 500mV, closed loop gain (R_f/R_i) = 10, input impedance = 50K ohms. Calculate maximum input offset errors for a temperature range of 0 to 50°C and for supply voltage regulation of 0.5% over a period of one day. Assume that initial input offset is adjusted to zero at 25°C and that the operational amplifier has the following drift coefficients:

$$\frac{\Delta e_{os}}{\Delta T} = \pm 20\text{uV}/^\circ\text{C} \qquad \frac{\Delta i_{os}}{\Delta T} = \pm 1\text{na}/^\circ\text{C}$$

$$\frac{\Delta e_{os}}{\Delta V^+} = \pm 20\text{uV}/\% \qquad \frac{\Delta i_{os}}{\Delta V^+} = \pm 2\text{na}/\%$$

$$\frac{\Delta e_{os}}{\Delta t} = \pm 50\text{uV/day} \qquad \frac{\Delta i_{os}}{\Delta t} = \pm 5\text{na/day}$$

Solution: R_i = 50K ohms, R_f = 500K ohms

$$e_{os} = \pm\left(\frac{20\text{uV}}{^\circ\text{C}}\right)25^\circ\text{C} \pm \left(\frac{20\text{uV}}{\%}\right).5\% \pm \left(\frac{50\text{uV}}{\text{day}}\right)(1\text{day}) = \pm 560\text{uV}$$

$$i_{os} = \pm\left(\frac{1\text{na}}{^\circ\text{C}}\right)25^\circ\text{C} \pm \left(\frac{2\text{na}}{\%}\right).5\% \pm \left(\frac{5\text{na}}{\text{day}}\right)(1\text{day}) = \pm 31\text{na}$$

Input Offset Error

$$\Delta V_s = e_{os} \frac{R_f + R_i}{R_i} + R_i I_{os} = \pm 2.2\text{mV}$$

$$\%\ \text{error} = \frac{\Delta V_s}{V_s} = 0.44\%$$

NON-INVERTING AMPLIFIER

The offset behavior of the non-inverting amplifier can be predicted by the circuit in Figure 5 where again the voltage and current offset are referred to the source voltage. R_s is the source impedance.

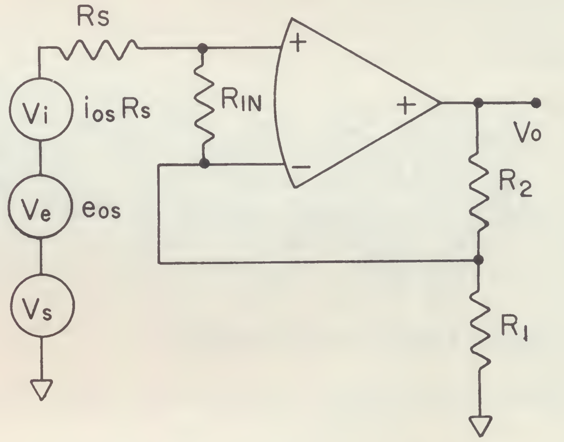


Fig. 5 — Non-Inverting Amplifier

For this circuit the following points should be noted:

1. Unlike the inverting amplifier, voltage offset referred to the source voltage is independent of closed loop gain. Thus, there is no increase in voltage drift (and noise) at unity or low values of closed loop gain.
2. As for the inverting amplifier, voltage and current offset referred to the source voltage is completely unaffected by the value for R_{IN}.
3. The effect of current offset referred to the source voltage is directly proportional to the source impedance, R_s. (In parallel with any other impedances to ground such as biasing networks.)
4. Unlike the inverting amplifier, very large input impedance can be obtained without increasing offset errors.

CURRENT TO VOLTAGE AMPLIFIERS

Many devices such as photocells and photomultipliers produce an output current from a relatively high source impedance. These devices can best be characterized by a current source as shown in Figure 6. In this circuit configuration the operational amplifier converts the input current to an output voltage with a low output impedance. Gain is proportional to R_f.

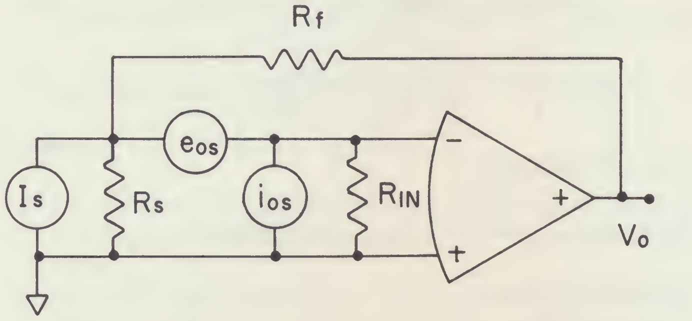


Fig. 6 — Current To Voltage Converter

In analyzing this circuit, it is more revealing to refer the voltage and current offsets to the signal source as current sources as shown in Figure 7.

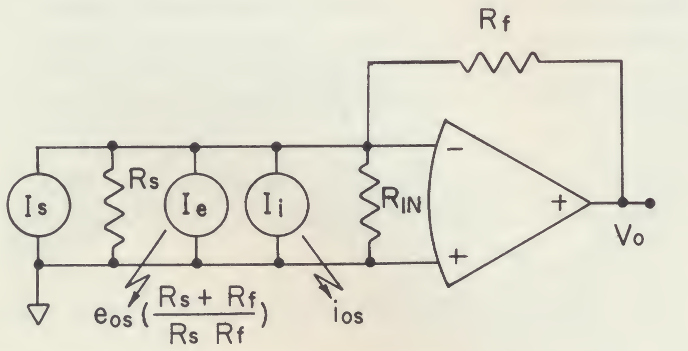


Fig. 7 — Offset Errors As Current Sources

Thus the offset errors referred to the signal source are:

$$\Delta I_s = e_{os}\frac{R_s + R_f}{R_s R_f} + i_{os}$$

To refer the signal and offset errors to the output we multiply by closed loop gain,

$$V_o = \left[-I_s R_f - e_{os}\frac{R_s + R_f}{R_s} - i_{os}R_f\right]\left[\frac{1}{1 + \frac{1}{A}\left(1 + \frac{R_f}{R_{IN}\,||\,R_s}\right)}\right]$$

From this analysis we can draw the following conclusions:

1. Open loop input impedance, R_{IN}, has no bearing on signal to offset ratio (or signal to noise ratio) referred to either the signal source or the output.
2. For $R_s \gg R_f$, which is generally the case for a high impedance current source, voltage offset (and noise) is not amplified referred to the output and therefore can often be ignored as compared to the effect of offset current.
3. Referred to the output, offset current like signal current is multiplied by R_f and the principle error is usually the ratio of offset current (and noise) to signal current.

EQUIVALENT CIRCUIT FOR DIFFERENTIAL INPUT AMPLIFIERS

Thus far, we have been discussing offset behavior for single - ended amplifiers. There are additional considerations for differential type amplifiers since each input has its own offset current source. Differential amplifiers depend on symmetry of the input circuitry for their proper operation and therefore it is reasonable to expect that the offset current at each input would be about equal and that changes in offset current would tend to track for changes in ambient temperature and supply voltage. This fact can be used to minimize input offset errors as we shall discuss.

Figure 8 shows the equivalent circuit for a differential amplifier.

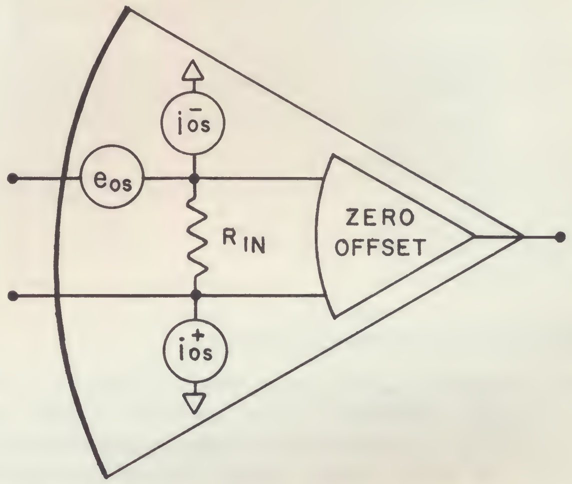


Fig. 8 — Equivalent Circuit For Differential Amplifier

We must now define another term, differential offset current, as follows:

$$i_{osd} = (i_{os}^- - i_{os}^+) = (I_{os}^- - I_{os}^+) + \frac{\Delta(i_{os}^- - i_{os}^+)}{\Delta T}\Delta T + \text{etc.}$$

where

1. $(I_{os}^- - I_{os}^+)$ is the initial difference in offset current at each input required to zero the output usually specified at 25° C with nominal supply voltage.
2. $\Delta(i_{os}^- - i_{os}^+) / \Delta T$ is the differential offset current temperature drift coefficient.

For transistor type differential amplifiers, offset current at each input as well as drift of offset current with temperature tends to track to within 20% to 30%. Or in other words, offset current at each input is about 3 to 5 times greater than the differential offset current. At this point, we should mention that there is great confusion between the definitions used

by discrete component manufacturers and integrated circuit manufacturers of operational amplifiers. Discrete component manufacturers such as Philbrick, Burr-Brown, Nexus and Analog Devices' use the definitions given here in specifying offset current.

Integrated circuit manufacturers define current at each input (i_{os}^- and i_{os}^+) as input bias current while they call differential input current ($i_{os}^- - i_{os}^+$) input offset current. Thus specifications for offset current and offset current drift can differ by 3 to 5 times depending on the definitions used.

Initial offset current also bears further discussion. It is possible to reduce initial offset current at a given temperature and supply voltage arbitrarily close to zero by using networks internal to the amplifier to supply a biasing or compensating current. This adjustment procedure will have no effect on the drift coefficients of offset current. In a few applications a very low value for initial offset current is a definite requirement. However, in most applications, initial offset current is of no consequence since it can be compensated for by external circuitry, in which case offset current drift is the only source of error.

CLOSED LOOP OFFSET PERFORMANCE OF DIFFERENTIAL INPUT AMPLIFIERS

Since offset current at each input tends to be equal, if we equalize the impedance of each input to ground, we tend to cancel the errors due to offset current. For example, the simple inverting amplifier is shown in Figure 9 with an offset current compensating resistor, R_c, in the non-inverting input. We have used the equivalent circuit of Figure 8 and have referred all of the offset errors to the source voltage. The by-pass capacitor, C, which is used to prevent loss of open loop gain at high frequencies, is optional.

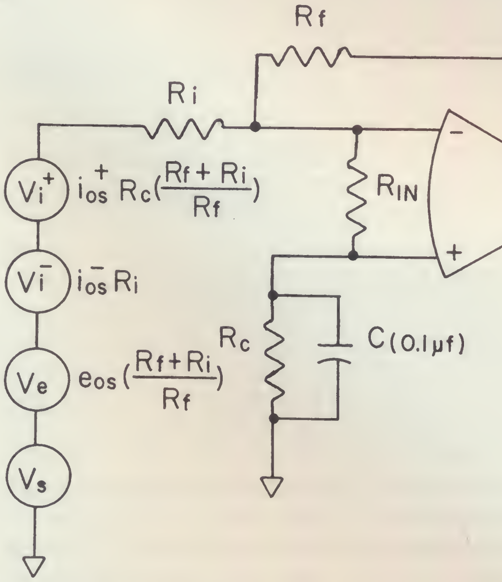


Fig. 9 — External Offset Current Compensation

If we set $R_c = R_iR_f/R_i+R_f$ then the total input offset error is,

$$\Delta V_s = e_{os}\frac{R_f + R_i}{R_f} + R_i\,(i_{os}^- - i_{os}^+)$$

Thus by equalizing the impedance at each input, offset behavior is then determined by differential offset current which is generally 3 to 5 times less than offset current.

INITIAL OFFSET ADJUSTMENTS

It is generally desirable or necessary to have some provisions for adjusting the initial input offset to zero. For the inverting amplifier, assuming $R_f >> R_i$, we know that initial offset errors referred to the source voltage are:

$\Delta V_s = E_{os} + R_i I_{os}$ (for single-ended amplifier or with $R_c = o$)

$\Delta V_s = E_{os} + R_i(I_{os}^- - I_{os}^+)$ (for differential amplifier with $R_c = R_i \| R_f$)

Most operational amplifiers have provisions for adding an external potentiometer to zero initial offset voltage, E_{os}. This adjustment will also zero errors due to initial offset current by unbalancing the input circuit of the amplifier to generate an equal and opposite voltage to compensate for ($R_i\ I_{os}$). However, it is bad practice to use the voltage offset potentiometer to balance the amplifier when the initial offset, ΔV_s, is predominately due to offset current (more precistely when $R_i I_{os}$ or $R_i\,(I_{os}^- - I_{os}^+)$ is greater than 4 - 5 millivolts). The reason is that a large unbalance of the input stage of the amplifier, which may be required to compensate for offset current, can degrade the temperature drift performance of the amplifier.

For the case where $I_{os}R_i$ or $(I_{os}^- - I_{os}^+)\ R_i >> E_{os}$ the voltage offset balance potentiometer should be replaced by a fixed resistor and an adjustable bias current should be summed as shown in Figure 10. Note that this current bias adjustment will zero both voltage and current offset for a fixed source impedance. For the exotic case where a precise input zero must be maintained under conditions of varying source impedance then both the current bias adjustment and the voltage offset potentiometer must be used to zero both E_{os} and I_{os} independently.

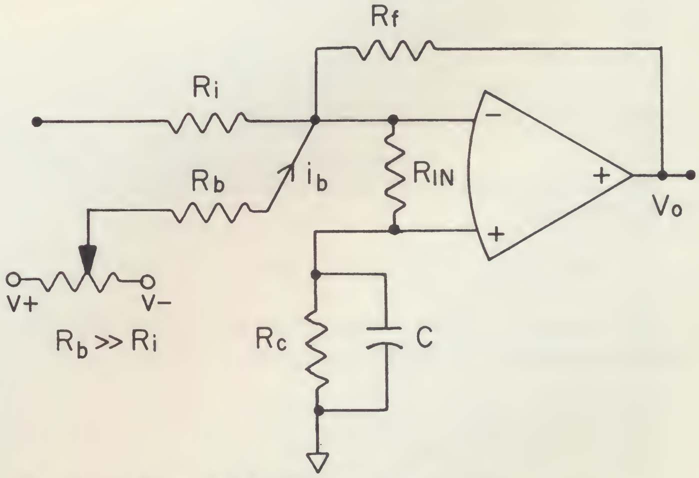


Fig. 10 — External Offset Current Bias Circuit

The non-inverting amplifier presents another problem when an external current bias circuit is used.

Usually the non-inverting amplifier is used to obtain very large input impedance. If we used the circuit in Figure 10 to supply offset current to the signal input we would lower the input impedance. A preferable circuit is shown in Figure 11 where the biasing network does not effect the input impedance.

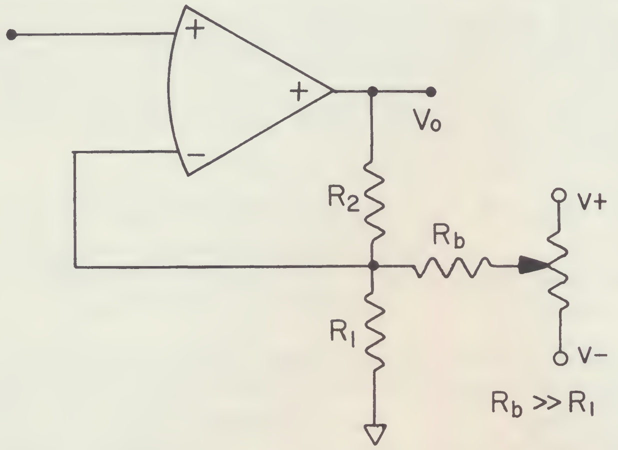


Fig. 11 — Bias Circuit For Non-Inverting Amplifier

TEST CIRCUIT FOR OFFSET VOLTAGE AND CURRENT

A convenient circuit for measuring offset parameters is shown in Figure 12.

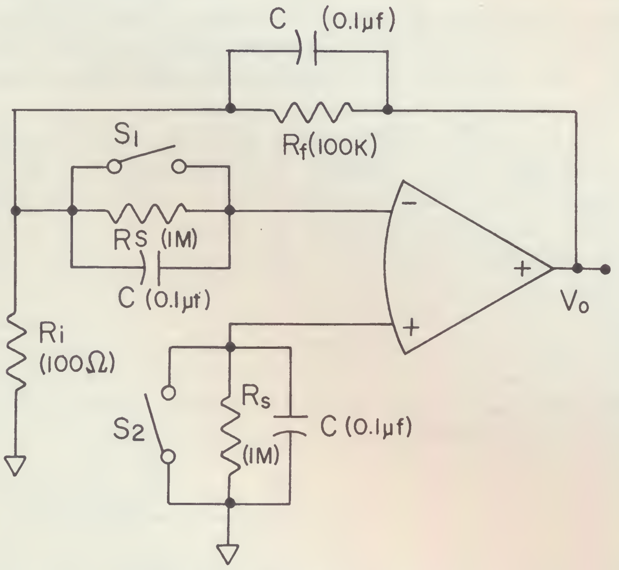


Fig. 12 — Test Circuit For Offset Parameters

The output voltage for this configuration, assuming $R_f >> R_i$, is,

$$V_o = - R_f/R_i\ (e_{os} + i_{os}^- R_s - i_{os}^+ R_s)$$

The various offset parameters are measured as follows assuming that $R_s >> e_{os} / (i_{os}^- - i_{os}^+)$:

1. Voltage Offset, e_{os}, - Close S_1 and S_2
   $V_o = - R_f/R_i\ e_{os}$
2. Offset Current, i_{os}^- - Close S_2, Open S_1
   $V_o = - R_f/R_i\ R_s\ i_{os}^-$
3. Offset Current, i_{os}^+ - Close S_1, Open S_2
   $V_o = - (R_f + R_i/R_i) R_s\ i_{os}^+ \approx R_f/R_i\ R_s\ i_{os}$
4. Differential Offset Current, $(i_{os}^- - i_{os}^+)$, - Open S_1 and S_2
   $V_o = - R_f/R_i\ R_s\ (i_{os}^- - i_{os}^+)$

The various offset coefficients are measured by varying a parameter such as temperature or supply voltage and recording the output voltage for the different switch positions.

OTHER DRIFT CONSIDERATIONS

Drift performance of differential operational amplifiers depends on the cancellation of temperature effects in matched components presumed to be at precisely the same temperature. Thermal gradients in the vicinity of the amplifier can cause input offsets an order of magnitude greater than predictable from the specifications. For example, a difference in temperature of only .01C between the junctions of two otherwise perfectly matched transistors in the input stage produces an input offset of 24uV. For this reason, over a narrow range of operating temperature, the input offset performance of differential amplifiers is more sensitive to thermal gradients than to actual change in ambient temperature. Over large changes of ambient temperature, thermal gradients are proportionately less significant in their effect on input offset although quite large offset transients can occur during large step changes in temperature due to non-uniform temperature rise. In critical applications in non-uniform temperature environments a shield or insulator should be used around differential amplifiers to create an isothermal surface.

One of the important but less obvious advantages of chopper stabilized operational amplifiers is that their drift performance does not depend on the cancellation of temperature effects in matched components and therefore offset performance is relatively immune to thermal gradients.

Another anamoly in specifying drift performance is that the temperature drift coefficients are generally specified as the average drift over a given temperature range. This is done for two reasons: first, a relatively large increment in temperature is required to eliminate the effects of thermal gradients from the measurements and secondly, it is not economical to record data and compute the drift coefficients for a large number of temperature increments. Figure 13 shows a typical graph of offset voltage vs. temperature as compared to the average drift coefficient. At the extremes of temperature the actual slope (uV/° C) may exceed the average slope, while in the vicinity of room temperature the actual slope may be less. It is also possible that the slope can be in either direction and in some cases the actual curve can slope up (or down) at both extremes of temperature.

Actually, a less misleading method of specifying offset performance would be to state the offset voltage change over a given temperature range.

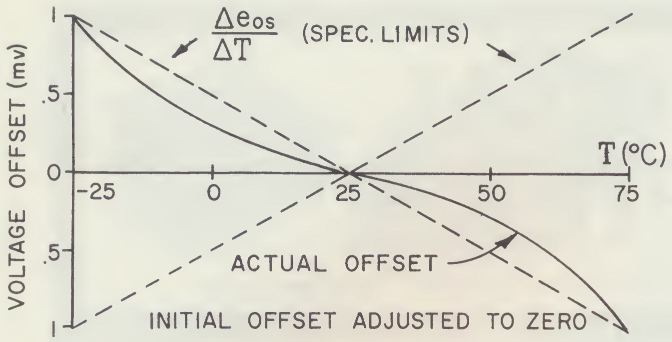


Fig. 13 — Voltage Offset vs. Temperature

Self-heating of the amplifier module following the application of power supply voltages can cause a change in initial offset voltage and current. The magnitude and duration of this warm up drift depends on the size and thermal mass of the module , the output voltage and current ratings and the arrangement of the components in the amplifier layout. In general this effect is more severe for large output voltage and current amplifiers which is one reason to consider the use of a separate booster amplifier so that the large temperature changes in the output stage are physically separated from the sensitive input transistors. Warm up offset voltage changes of 100 uV to 1 mV are possible over a time period of 15 to 20 minutes or longer.

Another source of input offset , which is sometimes overlooked , is due to rectification of high frequency overdrive signal. The specification for full output voltage or power response is usually regarded as a limitation on the output slewing rate capabilities of the amplifier. However, another reason for this specification is that input offsets can be generated when the the input signal contains frequency components which exceed the full output response specification. This accounts for the fact that the full output response capability of an amplifier can sometimes be less than that which can be predicted from the slewing rate specification.

TYPICAL DRIFT PERFORMANCE

At least four basic types of operational amplifiers are now commercially available to meet an extremely wide range of requirements for offset and drift performance. The table in Figure 14 gives some indication of the range of specifications which can be achieved with the various amplifier types.

Transistor Differential - The performance of transistor differential operational amplifiers is quite adequate for the vast majority of applications. Due to their relatively low cost and the versatility of the differential input design, these units are by far the most widely used. Since the offset current drift is relatively high, the impedance of the external input circuit should not be much greater than 100K ohms. Where long term offset stability over several months is important, metal film resistors should be used in the design of the input stage of the amplifier.

F.E.T. Differential - The primary advantage of FET amplifiers is their lower initial offset current and their lower offset current drift. This allows many megohms to be used in the external input circuit without excessive drift. Voltage offset drift, on the other hand, both with time and temperature is not so good for FET's as for transistors and these devices are more expensive.

Chopper Stabilized - Chopper Stabilized amplifiers are superlative in both offset voltage and current drift with time and temperature. Precision integration is one application which requires both very low voltage and current offsets. Signals in the low microvolt region can be successfully amplified with chopper stabilized amplifiers. Unlike differential type amplifiers, chopper stabilized amplifiers are relatively immune to offsets due to thermal gradients. Most of these devices have single - ended inputs which limits their application to the inverting connection.

Varactor Bridge (or Parametric) - The varactor bridge amplifier achieves offset current and drift of one to two orders of magnitude lower than FET's. As for FETs, offset voltage drift performance is only moderate. This amplifier is useful in electrometer applications where voltages and currents must be measured from source impedances in the range from 10^8 to 10^{12} ohms. Integrators with time constants of several hours can be designed. Low frequency noise is exceptionally good since 1/f noise is virtually eliminated.

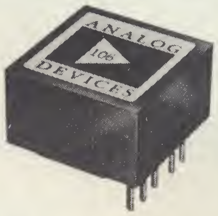
	$\frac{\Delta e_{os}}{\Delta T}$ uV/°C	$\frac{\Delta e_{os}}{\Delta t}$ uV/day	$\frac{\Delta i_{os}}{\Delta T}$ pa/°C	$\frac{\Delta i_{os}}{\Delta t}$ pa/day	I_{os} pa
Differential Transistor	3 to 30	5 to 100	200 to 2000	50 to 5000	1000 to 200,000
Differential F.E.T.	15 to 50	25 to 100	*	.1 to 1	50 to 150
Chopper Stabilized	0.2 to 5	0.5 to 10	0.5 to 10	0.5 to 10	10 to 100
Varactor Bridge	30 to 100	50 to 100	*	.01 to .1	1 to 10

*I_{os} doubles every 10°C, 1pa=10^{-12}amps

Fig. 14 — Typical Drift Performance

ANALOG DEVICES

OPERATIONAL AMPLIFIERS



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	HIGH PERFORMANCE DIFFERENTIAL			*LOW COST DIFFERENTIAL*		
	Excellent time drift, low initial voltage offset, high input impedance, low input current, high gain and selection of voltage drifts to 5uV/°C			For greatest economy without the usual sacrifice in gain, drift and output current. AC gain of 94db to 1KC on 106/107.		
SPECIFICATIONS (typical @ 25°C unless otherwise noted.)	**101 A/B/C** Wideband Inverting ±8 to 16V Power Supply 5ma Output Current	**102 A/B/C** Wideband Noninverting Very High Gain—20ma Fast Slewing Rate	**103 A/B/C** Low Frequency 20ma Output Current ±8 to 16V Power Supply	**106/L106** 5ma Output Current High Gain Excellent AC ampl.	**107/L107** 5ma Output Current High Gain Reduced Input Current	**108/L108** Low Frequency Lowest Input Current High Input Impedance
OPEN LOOP GAIN @ DC, rated load, min.	10^5	2×10^6	10^5	1.5×10^5	1.5×10^5	5×10^4
RATED OUTPUT						
Voltage, min.	±11V	±11V	±11V	±10V	±10V	±10V
Current, min.	5ma.	20ma.	20ma.	5ma.	5ma.	2.5ma
FREQUENCY RESPONSE						
Unity gain, small signal	10mc	10mc	500KC	1.5mc	1.5mc	500KC
Full Output Voltage	30KC	300KC	2KC	20KC	20KC	2KC
Slewing Rate	2V/μsec	30V/μsec	0.13V/μsec	1.2V/μsec	1.2V/μsec	0.12V/μsec.
Overload Recovery	200μsec	—	5msec.	1msec	1msec	5msec
INPUT VOLTAGE OFFSET						
Initial Offset, @ 25°C, max.[1]	±1mV	±1mV	±1mV	—	—	—
Avg. vs. temp., max.[5]	Models A — 20μV/°C, B — 10μV/°C, C — 5μV/°C			20μV/°C	20μV/°C	20μV/°C
vs. supply voltage, max.	15μV/%	10μV/%	15μV/%	20μV/%	20μV/%	20μV/%
vs. time	10μV/day	10μV/day	10μV/day	50μV/day	50μV/day	50μV/day
INPUT CURRENT OFFSET						
Initial Offset, @ 25°C, max.	±2na	±2na	±2na	±150na	±20na.	±2na
Avg. vs. temp., max.[5]	0.2na/°C	0.4na/°C	0.2na/°C	1.5na/°C	1.5na/°C	0.3na/°C
vs. supply voltage.	0.15na/%	0.15na/%	0.15na/%	2na/%	2na/%	0.3na/%
INPUT IMPEDANCE						
Between Inputs	4MΩ	6MΩ	4MΩ	100KΩ	100KΩ	4MΩ
Common Mode	500MΩ	500MΩ	500MΩ	50MΩ	50MΩ	500MΩ
INPUT VOLTAGE						
Max. Between Inputs	±15V	±15V	±15V	±15V	±15V	±15V
Max. Common Mode	±10V	±10V	±10V	±10V	±10V	±10V
Common Mode Rejection	20,000	20,000	20,000	20,000	20,000	20,000
INPUT NOISE						
Voltage, DC to 1CPS, P to P	—	—	—	—	—	—
5 to 50KC, RMS	4μV	8μV	4μV	4μV	4μV	4μV
Current, DC to 1CPS, P to P	—	—	—	—	—	—
POWER SUPPLY						
Voltage	±(8 to 16) VDC[2]	±(15 to 16) VDC	±(8 to 16) VDC[2]	±(15 to 16) VDC	±(15 to 16) VDC	±(15 to 16) VDC
Current, rated load	20ma.	35ma.	30ma.	15ma.	15ma.	5ma.
CASE SIZE	Fig. 1	Fig. 1	Fig. 1	Fig. 2/Fig. 1	Fig. 2/Fig. 1	Fig. 2/Fig. 1
PRICE	A B C	A B C	A B C	106 L106	107 L107	108 L108
1-9	$68 78 98	95 105 120	74 84 104	26 30	31 35	35 40
10-24	$66 75 95	92 102 116	71 81 101	25 29	30 34	33 37

NOTES

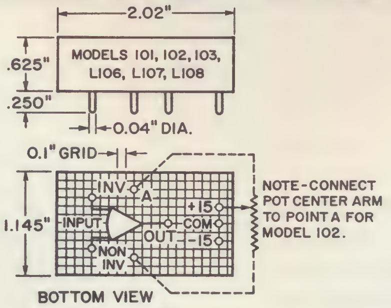
Note 1 — Adjustable to zero with external pot

Note 2 — Specifications given for ±15VDC

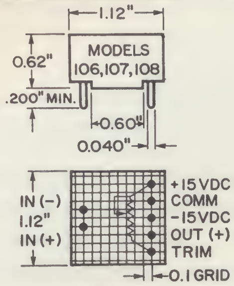
Note 3 — Maximum operating and storage temperature is 75°C

Note 4—0.06pa/°C from 0 to 50°C

Note 5 — Averaged over —25 to +85°C

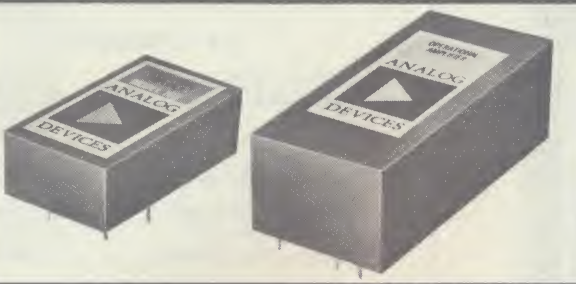


BOTTOM VIEW
FIGURE I



BOTTOM VIEW
FIGURE 2

WRITE FOR FOURTEEN PAGE MANUAL / DESCRIBING THEORY & APPLICATIONS OF OPERATIONAL AMPLIFIERS



ANALOG DEVICES

ALL SILICON OPERATIONAL AMPLIFIERS

HIGH OUTPUT CURRENT		*CHOPPER STABILIZED*				*ULTRA LOW INPUT CURRENT*
Output current of 100ma and bandwidth to 10mc drives galvonometers and coaxial cables.		Miniature encapsulated modules for P.C. mounting or plug-in sockets. Includes internal chopper drive and fast overload recovery circuitry. Very high gains and output current.				
113 High Gain Low Drift High Input Impedance	**116** Low Noise Excellent AC ampl. Fast Recovery	**201** 100ma Output Current Wideband Ultra Low Drift	**202** Wideband — 20ma Fast Slew Rate Ultra Low Drift	**203** Low Noise — 20ma Low Frequency Ultra Low Drift	**210** Low Cost — 20ma Very Fast Slew Rate Low Noise	**301** High CM Voltage Very High Zin Very Low Noise
2 x 10^6	10^5	10^9	10^9	10^8	10^8	10^6
±11V 100ma	±11V 100ma.	±11V 100ma.	±11V 20ma.	±11V 20ma.	±10V 20ma.	±10V 20ma.
10mc 300KC 30V/μsec —	10mc 500KC 30V/μsec 0.2μsec	10mc 500KC 30V/μsec 0.5μsec.	10mc 500KC 30V/μsec 0.5μsec.	2mc 20KC 1.2V/μsec 5μsec.	20mc 500KC 100V/μsec 0.2μsec.	500KC 5KC 0.3V/μsec 200μsec
±1mV 20μV/°C 2μV/% 10μV/day	±10mV 100μV/°C — —	±20μV 0.2μV/°C[3] 0.4μV/% 1μV/day	±20μV 0.2μV/°C[3] 0.4μV/% 1μV/day	±20μV 0.2μV/°C[3] 0.4μV/% 1μV/day	±100μV 1μV/°C 10μV/% 1μV/day	— 30μV/°C 30μV/% —
±1na 0.2na/°C —	±300na. 40na/°C —	50pa 0.5pa/°C[3] 1pa/%	50pa 0.5pa/°C[3] 1pa/%	50pa 0.5 pa/°C[3] 1pa/%	100pa. 2pa/°C 10pa/%	±1pa 0.3pa/°C[4] .001pa/%
7 MΩ 500MΩ	20KΩ 2.5MΩ	220KΩ N.A.	220KΩ N.A.	220KΩ N.A.	500KΩ N.A.	10^{10}Ω, 500pf 10^{12}Ω, 10pf
±15V ±10V 20,000	±15V ±10V —	±15V single ended	±15V single ended	±15V single ended	±15V single ended	±20V ±300V 10^8
— 8μV —	— 3μV —	25μV 10μV 20pa	25μV 10μV 20pa	10μV 10μV 10pa	5μV 10μV 10pa	1μV — .01pa
±(15 to 16) VDC 150ma.	±(15 to 16) VDC 150ma.	±(15 to 16) VDC 150ma.	±(15 to 16) VDC 50ma.	±(15 to 16) VDC 50ma.	±(15 to 16) VDC 60ma.	±(15 to 16) VDC 35ma.
Fig. 3	Fig. 4	Fig. 5	Fig. 5	Fig. 5	Fig. 5	Fig. 5
$195 $ 185	98 95	270 256	235 224	215 205	157 148	198 193

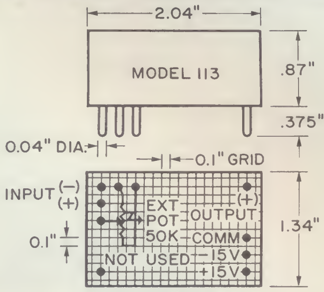


FIGURE 3

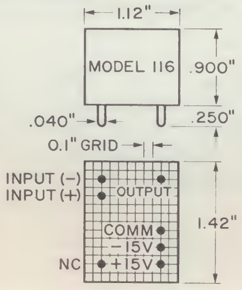


FIGURE 4

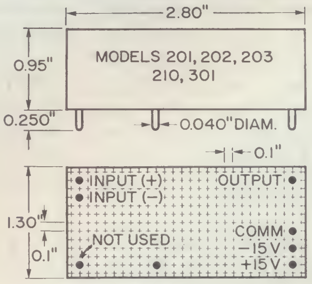
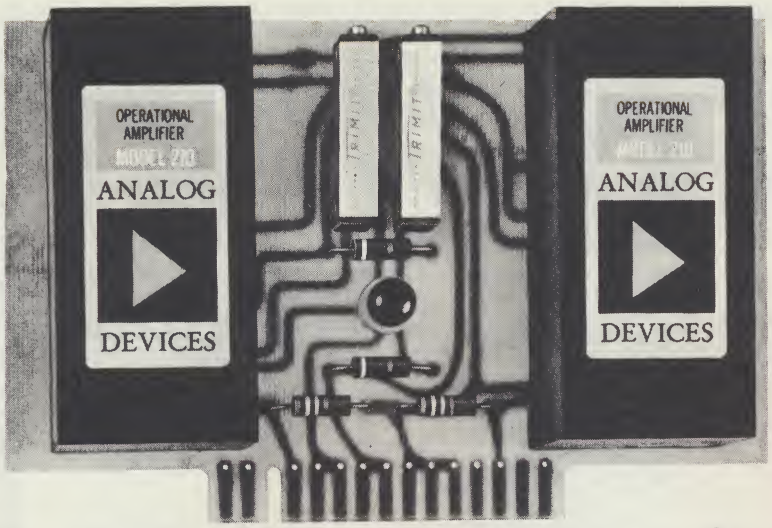


FIGURE 5

WRITE FOR ANALOG DEVICES' COMPLETE DATA ON ALL OF AMPLIFIERS ILLUSTRATED



Drift of only 1 µV/°C and 2 pa/°C

at a price you can afford

$157 Chopper Stabilized Operational Amplifier

For little more than the cost of a differential op amp you can reach right down into microvolt signals with orders-of-magnitude better stability and accuracy. Model 210 mounts right onto your P-C card, provides 100 volt/µsec slewing-rate, only 3 µV peak-to-peak noise

SPECIFICATIONS (Model 210)

DC Gain	Max Drift	Noise DC-2cps	Bandwidth	Slewing Rate	Max Offset	Output Rating	OEM Price
160 db	1 µV/°C 2 pa/°C	3 µV peak-peak	20 Mc	100 V/ µSec	50µV 50 pa	± 10 V @ 20 ma	$128 (100 lot)

Isn't that a spec-and-a-half for only $157? Well there's more yet. This new 3 cubic-inch op amp has built-in chopper-drive, plus an internal 0.2 µsec fast overload recovery network. Output is shortproof too.

No more AC chopper-excitation voltages, no more plug-and-socket interconnections, no long wires to suck up noise on their way to the summing junction, no problem of finding P-C card "floor-space" for an external overload recovery circuit. In many applications, the 50 µV & 50 pa offsets even let you eliminate the external balance potentiometer.

This is an excellent amplifier for such applications as precision integrators, low-level DC amplifiers, fast A-D and D-A converters, accurate pulse amplifiers, and many precision circuits in high-speed analog computers.

DRIFT 0.2 µV/°C — If you need even more exotic performance, our Model 203 has 0.2 µV/°C & 0.5 pa/°C drift in the same miniature P-C mounting package. (Price $215)

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